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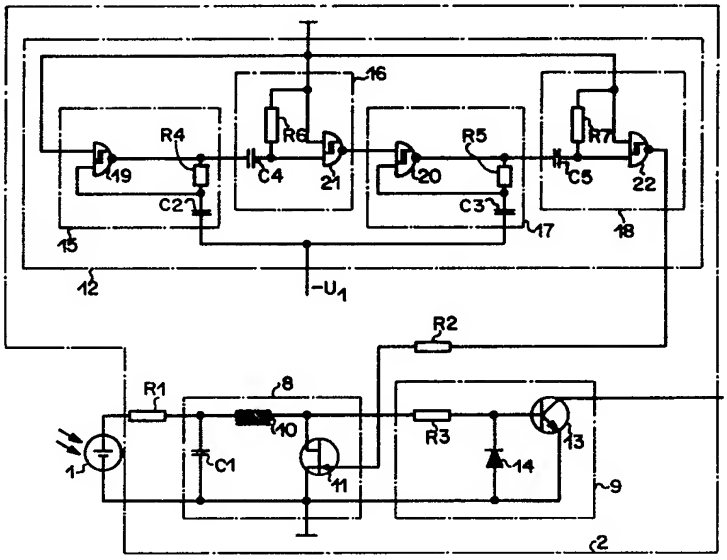
(54) **Signal reconditioning arrangements**

(57) A signal reconditioning arrangement (2) is operative to provide fail safe processing of a low *d.c.* voltage emitted by a sensor (1) – e.g. a photoelectric sensor – in the flame monitoring of oil or gas burners. In order to avoid drift problems, the *d.c.* voltage is not directly amplified. Instead, it is chopped by means of a controllable switch (11) and stepped up by an inductor (10). The energy stored by the sensor (1) in a capacitor (C1) is thus suppled to the inductor (10) in pulsed form. The switch (11) is controlled by a series of switching pulses from a pulse generator (12). The output of a Pi network (8), formed by the capacitor (C1), the inductor (10) and the switch (11), controls a semiconductor switch (13), which is operated in synchronism with the output pulses of the pulse generator (12). The pulse generator (12) comprises two astable multivibrators (15 and 17) and two monostable multivibrators (16 and 18), each of which comprises a two-input Schmitt trigger NAND-gate (19, 20, 21, 22) and an RC series combination or a CR network.

Fig. 2



GB 2 107 477 A

Fig. 1

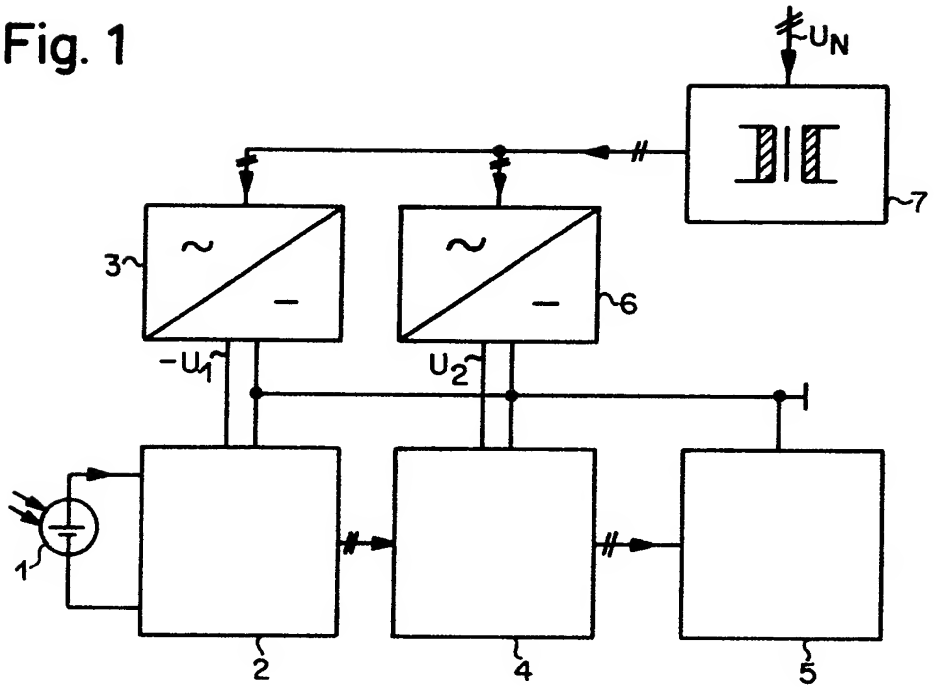

U_N
7
3
6
$-U_1$
U_2
1
2
4
5

Fig. 2

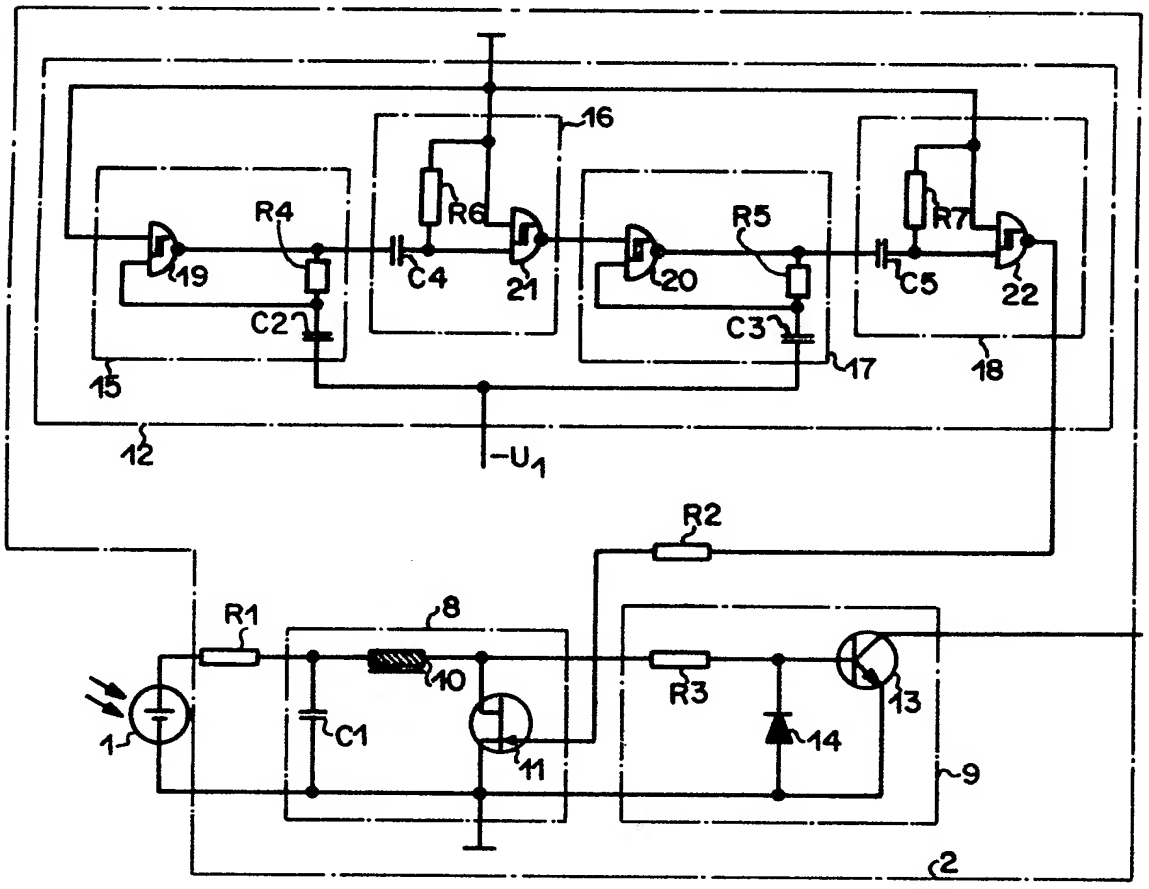
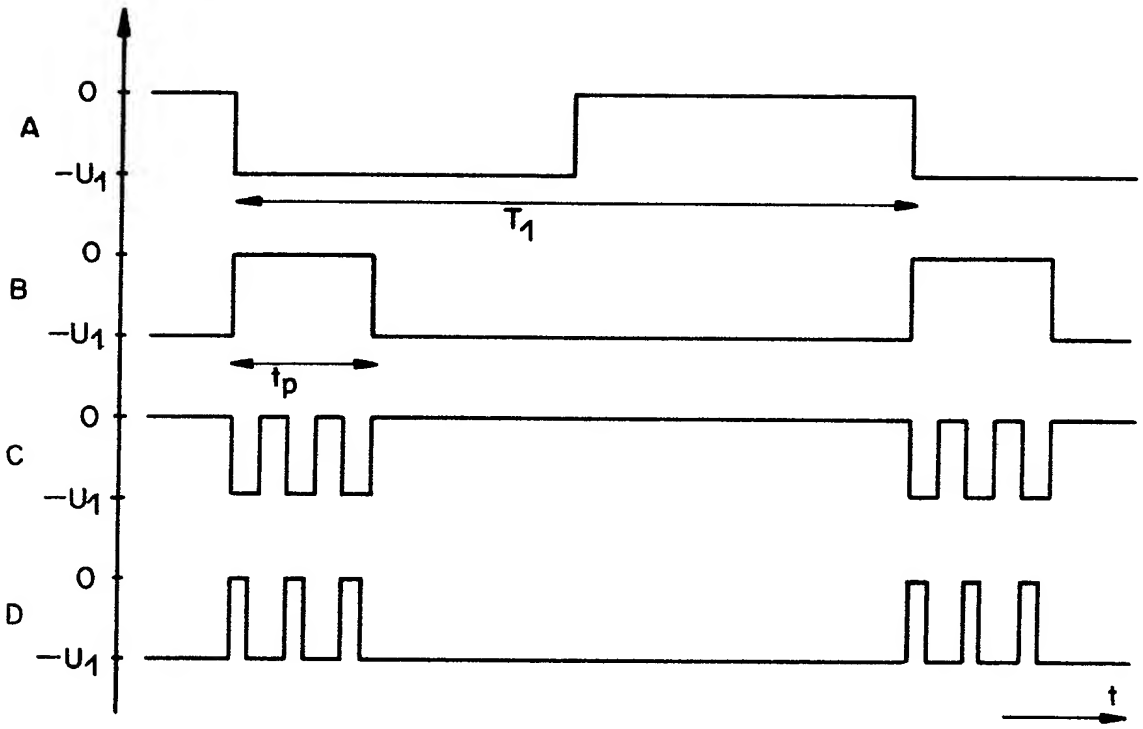

16
R4
R6
R5
R7
19
C4
21
20
C5
22
C2
C3
15
17
18
12
$-U_1$
R2
R1
8
10
R3
13
1
C1
11
14
9
2

Fig. 3



SPECIFICATION

Signal reconditioning arrangements

The invention relates to signal reconditioning arrangements for fail-safe processing of *d.c.* sensor voltages, that is signals from sensors operating with *d.c.* voltage.

Such sensors are used, for example, in flame monitors of oil or gas burners, for monitoring and indicating the presence of a flame. The flame monitors, together with their sensors, must be to a great extent intrinsically safe or fail safe, that is to say any possible defect in a component must be indicated by a "flame extinguished" signal.

It is known that self monitoring may be effected by first checking that the flame monitor is working properly each time the installation is put into operation. It is also known to use installations with two independently operating flame monitors and to monitor for their signalling permanent in the same sense.

In other known flame monitors, correct switching off of the monitor is checked by a testing cycle at certain intervals of time; a further relay takes over the supplying of a fuel valve and an additional electromagnet takes over the interruption of the sensor illumination during the testing interval. A flame monitor of the last type, including a signal reconditioning arrangement for fail safe processing of DC sensor voltages, has been proposed in our co-pending UK Patent Application Publication No. 2 078 415A and in corresponding Swiss Patent Application No. 4708/80-3.

All these solutions involve a relatively large outlay, and the last mentioned have the further disadvantage that the relays or electromagnets are operated at a high switching frequency in order to make the fault recognition time as short as possible.

According to the present invention there is provided a signal reconditioning arrangement for fail safe processing of *d.c.* sensor voltages wherein a *d.c.* voltage sensor is connected by a first resistor to a Pi network having an output connected to a control input of a first switch, the Pi network having an input cross arm that comprises a first capacitor, a line arm that comprises an inductor, and an output cross arm that comprises a second switch controlled by a pulse generator.

A signal reconditioning arrangement embodying the invention and described hereinbelow avoids at least to some extent the above-mentioned disadvantages in continuous operation, and is capable of controlling the flame relay circuit described above, or a similar arrangement, without any problems due to *d.c.* voltage drift arising.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which identical references denote identical components in all the figures, and in which:

Figure 1 is a block circuit diagram of a flame monitor;

Figure 2 is a circuit diagram of a signal reconditioning arrangement embodying the invention and incorporated in Figure 1; and

Figure 3 is a waveform diagram of a pulse generator of the arrangement of Figure 2.

Figure 1 shows a flame monitor that includes a sensor 1 that is operated by *d.c.* voltage or transmits *d.c.* voltage, and which will hereinafter be referred to in general terms as the *d.c.* voltage sensor 1. The sensor 1, which in this examplary arrangement is a photoelectric sensor, is illuminated by a flame of an oil or gas burner and feeds a signal reconditioning arrangement 2 through two terminals or poles. The arrangement 2 is supplied with a negative first *d.c.* supply voltage $-U_1$ through two terminals by a first supply unit 3 having its positive pole connected for example to earth potential. The signal reconditioning arrangement 2 in turn controls an input of a flame relay circuit 5 through two terminals via a relay switching amplifier 4. The amplifier 4 and circuit 5 are fed through two terminals by a common second supply unit 6 with a positive second *d.c.* supply voltage U_2. The negative pole of the supply unit 6 is connected to the positive pole of the negative first DC supply voltage - U_1. A mains *a.c.* voltage U_N feeds both supply units 3 and 6 through two terminals via a single phase transformer 7.

The DC voltage sensor 1 may for example be a cell which is sensitive to visible or ultra-violet (UV) light, its working voltage being too low to control directly a switching transistor.

Except for the signal reconditioning arrangement 2, the circuit components shown in Figure 1 are known from the prior art mentioned above. They will therefore not be explained in detail below. However, to clarify the position, it should be mentioned that the flame relay circuit 5 includes a flame relay and comprises two parallel current paths (not shown) of opposed polarity, which both have a common relay capacitor. The first current path, corresponding to the direction of flow of the positive second *d.c.* supply voltage U_2, comprises a series arrangement of the following components in the following order: a first diode, a holding coil or winding of the flame relay, a second diode and the common relay capacitor. The second current path comprises the relay capacitor, a third diode, an attracting coil or winding of the flame relay and a fourth diode, which again are all arranged in series in the order given above. The above-outlined flame relay circuit is described in greater detail in the above-mentioned copending UK Patent Application Publication No. 2 078 415A: see the components 35 to 41 in Figure 1 thereof.

The flame monitor shown in Figure 1 operates in the following manner. The low voltage of the *d.c.* voltage sensor 1 is converted in the signal reconditioning arrangement 2 into a series of switching pulses, which periodically short circuit the input of the relay switching amplifier 4 with the aid of an output switch. An output switch of the amplifer 4, which is for example a bipolar transistor, short circuits the flame relay circuit 5 in synchronism with or in the rhythm of the pulses. The two current paths of the flame relay circuit 5 are so arranged that only the second path can make the flame relay attract, while the first path merely supplies a holding current for the relay.

So long as the output switch of the signal reconditioning circuit 2 is open, the output switch of the relay switching amplifier 4 will be open and the common relay capacitor will be charged along the first current path. So long as a charging current is flowing the flame relay will be held, if it was attracted at the beginning of the charging process. The time between two charging process is chosen so that, when the circuit is in the correct state, the charging current of the relay capacitor will always just be sufficient to make the flame relay hold. In this example the maximum time between them can be 900 ms.

If the output switch of the circuit 2 is closed, that of the relay switching amplifier 4 will also be closed, the flame relay circuit will be short circuited and the common relay capacitor will be discharged along the second current path, thereby energising the flame relay. In its energised state a switching contact of the relay indicates the presence of a flame.

Thus, the relay capacitor is periodically charged and discharged by the output pulses of the signal reconditioning arrangement 2. However, this only takes place so long as all components are functioning correctly and the d.c. voltage sensor 1 senses a flame.

The discharging current of the relay capacitor should last for a predetermined time, e.g. approximately 50 ms. If it lasts considerably longer, possibly due to some fault, the capacitor will be over discharged and cannot then supply the holding current. Similarly, the discharge current must not flow for a period of substantially shorter duration, since the relay capacitor would otherwise be discharged to little and the charging current in the next charging phase would be too weak to hold the flame relay.

Figure 2 shows the *d.c.* voltage sensor 1 supplying the signal reconditioning arrangement 2. The sensor 1 has a first terminal or pole connected via a first resistor R1 to a first terminal or pole of the input of a Pi network 8, the output of which controls a control input of a first switch 9. The input cross arm of the Pi network 8 comprises a first capacitor C1, its line arm comprises an inductor 10 and its output cross arm comprises a second switch 11, a control input of which is connected by a second resistor R2 to an output of a pulse generator 12. The first switch 9 may for example comprise a bipolar semiconductor switch 13, the base of which acts as a control input and is controlled by a third resistor R3, with a voltage limiting diode 14 connected in parallel with the base-emitter junction. The cathode of the diode 14 is connected to the base of the bipolar semiconductor switch 13, while its collector forms a single pole output of the signal reconditioning arrangement 2. The switch 13 may for example be an NPN transistor. The second switch 11 may be an N-channel field effect transistor. The second terminal or pole of the *d.c.* voltage sensor 1, the junction of the first capacitor C1 and the second switch 11, the anode of the voltage limiting diode 14 and the emitter of the biplar semiconductor switch 13 are interconnected and applied to the positive pole of the negative first *d.c.* supply voltage $-U_1$, which may for example be connected to earth potential.

The pulse generator 12 comprises a first astable multivibrator 15, an output of which supplies a control input of a downstream first monostable multivibrator 16, an output of which in turn controls a clearing or enabling input of a downstream second astable multivibrator 17 of a higher frequency than the multivibrator 15. An output of the multivibrator 17 is connected to a control input of a downstream second monostable multivibrator 18, an output of which forms the output of the pulse generator 12.

The astable multivibrators 15 and 17 comprise, respectively, a first two-input Schmitt triger NAND -gate 19 and a second two-input Schmitt trigger NAND-gate 20. The gates 19, 20 are loaded, respectively, with a first RC series combination R4-C2 and a second RC series combination R5-C3, the common ends of the resistor and capacitor forming each RC series combination being coupled to a first input of the associated NAND-gate 19 or 20. The RC series combination R4-C2 comprises a fourth resitor R4 and a second capacitor C2, and the RC series combination R5-C3 comprises a fifth resistor R5 and a third capacitor C3. The output of the NAND-gate 19 is connected to the second end of the resitor R4 and forms the output of the multivibrator 15. The output of the NAND-gate 20 is connected to the second end of the resistor R5 and forms the output of the multivibrator 17. The second end of each of the capacitors C2 and C3 is connected to the negative pole of the DC supply voltage $-U_1$. The second inputs of the two NAND-gates 19 and 20 are the relevant clearing or enabling inputs; that of the NAND-gate 19 is applied permanently to earth potential (and thus to logic level "1") and the gate is thus permanently enabled.

The monostable multivibrators 16 and 18 comprise, respectively, a third Schmitt trigger NAND -gate 21 with a first CR network C4-R6 and a fourth Schmitt trigger NAND-gate 22 with a second CR network C5-R7. The common first ends of the resistor and capacitor forming each such CR network are joined to a first input of the associated NAND -gate 21 or 22, respectively. The CR network C4-R6 comprises a fourth capacitor C4 and a sixth resistor R6, and the second CR network C5-R7 comprises a fifth capacitor C5 and a seventh resistor R7. The control input of the monostable multivibrator 16 is coupled to the second end of the capacitor C4. The control input of the monostable multivibrator 18 is coupled to the second end of the capacitor C5. The second ends of the resistors R6 and R7 associated with the NAND-gates 21 and 22 are coupled to the positive pole of the *d.c.* supply voltage $-U_1$, which may for example be at earth potential.

The four Schmitt trigger NAND-gates 19, 20, 21 and 22 may, for example, comprise a CMOS Quad 2-input NAND Schmitt trigger, for example type MC 14093B, produced by Motorola.

The operation of the signal reconditioning arrangement of Figure 2 will now be described with reference to the waveform (pulse) diagrams of Figure 3. The astable multivibrator 15 constantly generates a low frequency square wave pulse train having a period T_1 which is, for example, equal to

500 ms. The pulses are shown at A in Figure 3 as a function of time *t*. The downstream monostable multivibrator 16 is triggered by the negative-going transitions or flanks of the output pulses of the astable multivibrator 15 and delivers a positive pulse with a duration t_p equal for example to 50 ms for each such negative-going transistion, such pulses having a repetition time of $T_1 = 500$ ms. This output signal of the monostable multivibrator 16 is shown at B in Figure 3, as a function of time *t*.

The second astable multivibrator 17 oscillates at a frequency approximately 1000 times greater than that of the output signal from the astable multivibrator 15, naturally only during enabling or clearing time intervals $t_p \simeq 50$ ms predetermined by the multivibrator 16; this signal from the multivibrator 17 is shown at C in Figure 3.

The second monostable multivibrator 18 is triggered by the negative-going transitions of the output pulses of the astable multivibrator 17. During the enabling time intervals $t_p \simeq 50$ ms the multivibrator 18 delivers short positive output pulses, in synchronism with its input frequency, with a sensing ratio of, for example, ½ to ⅓ of the period of the multivibrator 17, depending on the values of the capacitor C5 and resistor R7. These output pulses are shown at D in Figure 3. All the pulses shown in Figure 3 are at one or the other of the levels OV and $-U_1$. Part of the resistor R7 may possibly be short circuited by a switch (not shown), in order to increase sensitively at the input of the switching amplifier 4, since this makes the output pulses narrower and thus reduces energy withdrawal from the capacitor C_1.

In contrast with arrangements already known or proposed, in the illustrated arrangement the low *d.c.* voltage of the sensor 1 is not amplified directly as a *d.c.* voltage signal. Instead, it is chopped by means of the second controllable switch 11 and stepped up by means of the inductor 10. This eliminates the problem of drift which arises with *d.c.* voltage amplifiers which are otherwise required. The voltage generated by the *d.c.* voltage sensor 1 charges the capacitor C1. The energy thus stored is then taken from the capacitor C1 within a very short time and passed to the semiconductor switch 13 at a higher voltage level. This happens periodically, approximately twice per second. The output of the semiconductor switch 13 controls the downstream relay switching amplifier 4.

As a means of transferring the energy stored in the capacitor C1 to the control input of the semiconductor switch 13 with minimum loss, the voltage on the capacitor C1 is connected to and disconnected from the inductor 10 at high frequency, for about 50 ms each time, in the above-mentioned half-second rhythm. The advantage of using a high frequency is that the inductor 10 can be chosen to be very small. In addition, the pulses chosen to control the second switch 11 are asymmetric, so that the switched-on time is shorter than the switched-off time, which has a favourable effect on the efficiency of energy transmission.

In Figure 3, the control pulses are shown in a purely diagrammatic form at D.

During the time $t_p \simeq 50$ ms, when the output pulses of the pulse generator 12 are energising the second switch 11, the capacitor C1 is to a large extent discharged. The O pulses which arise at the output of the semiconductor switch 13 during this time are smoothed in the downstream relay switching amplifier 4, so that in the end a pulse lasting 50 ms is available for the flame relay circuit 5. As a means of obtaining this pulse periodically in the half-second rhythm, the capacitor C1 must thus repeatedly be charged to a sufficient degree, and this can only happen when the second switch 11 is open and the *d.c.* voltage sensor 1 is generating sufficient voltage. In theory, it would also be possible to generate a single pulse from the capacitor charge, and to trigger a monostable trigger circuit or tipping stage with it, such circuit then delivering the 50 ms pulse. However, control with a series of switching pulses provides greater safety from individual interference pulses, and the use of a single integrated component is quite obvious for the type of pulse reconditioning chosen. Other modifications of the circuit are possible within the scope of the invention.

If the second input is enabled, the signal at the first input of the Schmitt trigger NAND-gate 19 or 20 of the astable multivibrator 15 or 17, respectively, is inverted in the NAND-gate, delayed in the downstream RC series combination R4-C2 or R5-C3, respectively, then returned to the first input of the NAND-gate 19 or 20. Its input signal, and with it the output signal of the astable multivibrator 15 or 17, therefore changes its digital value with continuous time delays, and the circuit in question thus operates as a square wave signal generator.

When a negative-going transition appears at the control input of the monostable multivibrator 16 or 18, a charging current in pulse form flows through the capacitor C4 or the capacitor C5. It generates a negative voltage pulse in the downstream resistor R6 or R7, of a duration determined by the values of the capacitor and resistor in question, and the pulse is inverted to a positive voltage pulse at the downstream NAND-gate 21 or 22. Nothing happens in the case of positive-going transistions of the control input signal, since both poles of the capacitor C4 or C5 in question are then earthed.

CLAIMS

1. A signal reconditioning arrangement for fail safe processing of *d.c.* sensor voltages, wherein a *d.c.* voltage sensor is connected by a first resistor to a Pi network having an output connected to a control input of a first switch, the Pi network having an input cross arm that comprises a first capacitor, a line arm that comprises an inductor, and an output cross arm that comprises a second switch controlled by a pulse generator.

2. An arrangement according to claim 1, wherein the first and second switches are semiconductor switches.

3. An arrangement according to claim 2, wherein the second switch is an N-channel field effect transistor having a control input connected to be controlled by a second resistor.

4. An arrangement according to claim 2 or claim 3, wherein the first switch is a bipolar NPN transistor,

the base of which is connected to be controlled by a third resistor and the base-emitter junction of which has a diode connected in parallel with it, the cathode of the diode being connected to the base of the transistor.

5. An arrangement according to any one of the preceding claims, wherein the pulse generator comprises a first astable multivibrator having an output connected to an input of a downstream, first monostable multivibrator, an output of the first monostable multivibrator is connected to an enabling input of a downstream, second astable multivibrator operative at a higher frequency than the first astable multivibrator, an output of the second astable multivibrator is connected to an input of a downstream, second monostable multivibrator, and the duration of the output pulses of each monostable multivibrator is shorter than the period of its input signals.

6. An arrangement according to claim 5, wherein each of the two astable multivibrators comprises a two-input Schmitt trigger NAND-gate having an output loaded with an RC series combination, the common ends of the resistor and capacitor of each RC series combination are connected to a first input of the associated Schmitt trigger NAND-gate while the second end of the capacitor in question is connected to a negative pole of a negative *d.c.* supply voltage, the second input of each Schmitt trigger NAND-gate is an enabling input, and an input of the first astable multivibrator is permanently enabled by connection to a positive pole of the negative *d.c.* supply voltage.

7. An arrangement according to claim 5 or claim 6, wherein each of the two monostable multivibrators comprises a two-input Schmitt trigger NAND -gate, a first input of which is controlled by a CR network, the common ends of the capacitor and resistor of each CR network are coupled to the first input of the associated Schmitt trigger NAND-gate, and the second end of the resistor of each CR network and the second input of the associated Schmitt trigger NAND-gate are connected to a positive pole of a negative *d.c.* supply voltage.

8. A signal reconditioning arrangement substantially as herein described with reference to Figures 2 and 3 of the accompanying drawings.

9. Use of a signal reconditioning arrangement according to any one of claims 1 to 8 as part of a flame monitoring means for oil or gas burners.

10. A flame monitor incorporating a signal reconditioning arrangement according to any one of claims 1 to 8.

11. A flame monitor substantially as herein described with reference to Figures 1 to 3 of the accompanying drawings.

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ABSTRACT:

CHG DATE=19990617 STATUS=O> A signal reconditioning arrangement (2) is operative to provide fail safe processing of a low d.c. voltage emitted by a sensor (1) - e.g. a photoelectric sensor - in the flame

monitoring of oil or gas burners. In order to avoid drift problems, the d.c. voltage is not directly amplified. Instead, it is chopped by means of a controllable switch (11) and stepped up by an inductor (10). The energy stored by the sensor (1) in a capacitor (C1) is thus suppled to the inductor (10) in pulsed form. The switch (11) is controlled by a series of switching pulses from a pulse generator (12). The output of a Pi network (8), formed by the capacitor (C1), the inductor (10) and the switch (11), controls a semiconductor switch (13), which is operated in synchronism with the output pulses of the pulse generator (12). The pulse generator (12) comprises two astable multivibrators (15 and 17) and two monostable multivibrators (16 and 18), each of which comprises a two-input Schmitt trigger NAND-gate (19, 20, 21, 22) and an RC series combination or a CR network. □